**EAST WEST UNIVERSITY**

**Department of Computer Science and Engineering  
  
Semester:** Spring 2017  
**Course Number:** CSE345  
**Course Title:** Digital Logic Design

**Experiment Number:** 03  
**Experiment Title:** Behavioral Verilog Simulation of a Combinational Logic Circuit

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**Objectives:**

* To learn behavioral Verilog coding of a combinational logic circuits using procedural model.
* To learn behavioral Verilog coding of a combinational logiccircuits using continuous assign statement.

**Answer to the post-lab Question:**

**1.** F=A’B’C+A’BC’+AB’C’+A’BC

|  |  |
| --- | --- |
| A B C | F |
| 0 0 0 | 0 |
| 0 0 1 | 1 |
| 0 1 0 | 1 |
| 0 1 1 | 0 |
| 1 0 0 | 1 |
| 1 0 1 | 1 |
| 1 1 0 | 0 |
| 1 1 1 | 0 |

The simulation results agree with the truth table prepared.

**Conclusion:**

By doing this experiment, for combinational circuits and continuous assign statement we have written behavioral Verilog code and after then we simulated these using Quartus 2 software.